

REMARKS

Claims 1-23 are pending in the application. Claims 1-23 have been amended. The Examiner's reconsideration of the rejections is respectfully requested in view of the following remarks.

Claim Rejections - 35 U.S.C. § 102

Claims 1, 3, 4, 6 and 8 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,357,136 to Yoshioka, for the reasons set forth on pages 2-4 of the Office Action. In addition, claims 1 and 6-8 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,159,826 to Kim et al., for the reasons set forth on page 4 of the Office Action.

Applicants respectfully submit that at the very minimum, claim 1 is patentably distinct and patentable over both Yoshioka and Kim. Indeed, on a *fundamental* level, neither Yoshioka nor Kim discloses or suggests, for example, *a semiconductor IC chip comprising a bond pad that includes a probe area for providing contact with a probe for device testing, and a bond area for providing an attachment point for a bond wire, wherein the bond area is separate from the probe area*, as essentially claimed in claim 1.

Yoshioka Does Not Anticipate the Claimed Inventions

More specifically, with regard to Yoshioka, Examiner acknowledges on page 3 of the Office Action that "*Yoshioka is silent to the second portion including a probe area ...*" but then Examiner contends that "*the bond pad area can also function as the probe area, as evidenced by Applicants disclosure on page 3*". It is respectfully submitted, however, that such assertion misses the point and actually teaches away from the claimed invention.

Indeed, Applicant explains on page 3 of the specification that with prior art bond pads, the same surface of the bond pads are used for both probe contacts for testing and for bond wire connections, which can result in damage to the bond pad (e.g., adversely affecting bonding connections) and/or to underlying connections/structures. In stark contrast, the claimed inventions provide a solution to these problems by providing bond pads with separate probe areas and bond areas, which is clearly not disclosed or even remotely suggested by Yoshioka.

In particular, Yoshioka discloses in FIGs. 1 and 2(e), for example, an interconnection layer (19) that electrically connects a bond pad (30) to a diffusion (source/drain) region (3) of a transistor (25). The bond pad (30) is a portion of the interconnection layer (19) that is exposed through a bond pad opening (23) in an insulation layer (20). (See, e.g., Col. 4, lines 16-24; and Col. 5, lines 20-24).

The bond pad and connection framework disclosed by Yoshioka actually teaches away from the invention of claim 1 because contacting a probe to the bond pad (30) (i.e., the exposed surface of the interconnection layer (19)) can result in damage to the bond pad (30) or the structures/layers (15, 18) below the bond pad (30).

In any event, Yoshioka does not disclose or suggest *a bond pad having a first portion disposed over a metal line and an interconnect, and a second portion disposed over a dielectric layer and offset from the at least one metal line*, as essentially claimed in claim 1. Indeed, Yoshioka does not disclose or suggest in FIGs. 1 or 2e, for example, that the bond pad (30) has a second portion providing a separate probe area which is offset from a metal line (or layer) (15). In contrast, FIGs. 1 and 2e depict the bond pad (30) portion of the interconnect (19) being disposed over the metal layer (15), not offset from the metal layer (15). In such instance, as

noted above, probing the bond pad (30) could result in damage to the surface of the bond pad (30) as well as the underlying barrier layer (18) and metal layer (15).

For at least the above reasons, claim 1 is patentably distinct and not anticipated by Yoshioka. Moreover, claims 3, 4, 6 and 8 are patentably distinct and patentable over Yoshioka at least by virtue of their dependence from claim 1.

Kim Does Not Anticipate the Claimed Inventions

Furthermore, respect to claim 1, Kim does not disclose or suggest *a semiconductor IC chip having bond pads with separate areas for providing bonding and probing*, as essentially claimed in claim 1. In general, Kim discloses a method for wafer level testing wherein separate wafer probing pads (38) are formed in chip scribe line portions (34) of a semiconductor wafer (30), and wherein bond pads (36) are separately formed on the semiconductor IC chip (32) portions of the wafer (30) (see, e.g., FIGs. 3 and 4; Col. 3, lines 5-25). After wafer level testing wherein probes (60) are contacted to the wafer probe pads (38), the wafer (30) is cut along the scribe lines, which essentially results in removing the wafer probe pads (38) and forming semiconductor chips (32) having only bond pads (56a) (see, e.g., FIGs. 5 and 6; Col. 3, lines 25-58).

In other words, although Kim arguably addresses the problem of damage to bond pads by forming separate probe pads on the wafer, the method of Kim is essentially limited to wafer level probing because Kim teaches that the bond pads (56a) of the semiconductor chips (32) are not used for probing. This is in contrast to the claimed inventions which include *semiconductor IC chips having bond pads that provide separate areas for bonding and probing*. Advantageously, the claimed inventions provide semiconductor chips having bond pads that include separate probe areas, which enables testing of such chips on both wafer and chip levels.

Furthermore, Kim does not disclose or suggest *a bond pad having a first portion disposed over a metal line and an interconnect, and a second portion disposed over a dielectric layer and offset from the at least one metal line*, as essentially claimed in claim 1. Indeed, Kim does not disclose or suggest in FIGs. 6 or 9, for example, that the bond pad (56 or 56a) of the semiconductor chip (32) has a second portion providing a separate probe area which is offset from a metal line (or layer) (52a) or other components (e.g., P+ region). In the embodiments of FIGs. 6 and 9 of Kim, contacting a probe tip to the bond pad (56, 56a)) could result in damage to the surface of the bond pad as well as the underlying structures, as with the prior art bond pads.

For at least the above reasons, claim 1 is believed to be patentably distinct and patentable over Kim. Moreover, claims 6-8 are patentably distinct and patentable over Kim at least by virtue of their dependence from claim 1.

Moreover, although not specifically asserted as a rejection in the Office Action, Applicant respectfully submits that claim 18 is clearly patentably distinct and patentable over Kim and Yoshioka, either singularly or in combination, at least for the reasons given for claims 1 and 10 above.

Accordingly, withdrawal of the claim rejections under 35 U.S.C. § 102 is respectfully requested.

Claim Rejections - 35 U.S.C. § 103

The following claim rejections were asserted under 35 U.S.C. § 103(a):

(i) Claims 1, 3, 4, 6, 7, 10, 12, 15 and 15 stand rejected as being unpatentable over Kim in view of Yoshioka, for the reasons set forth on page 6 of the Office Action (although the rejection only addresses claim 4) ;

(ii) Claim 3 stands rejected as being unpatentable over Kim as applied to claim 1, in further in view of U.S. Patent No. 5,785,236 to Cheung or U.S. Patent No. 5,877,557 to Zawaideh, for the reasons set forth on page 5-7 of the Office Action;

(iii) Claims 3 and 5 stand rejected as being unpatentable over Kim or Yoshioka, as applied to claim 1, and further in view of U.S. patent No. 6,107,122 to Wood, for the reasons set forth on page 7 of the Office Action;

(iv) Claims 2-4 stand rejected as being unpatentable over Kim or Yoshioka, as applied to claim 1, and further in view of Applicant's Admitted Prior Art, for the reasons set forth on pages 7-8 of the Office Action;

(v) Claims 9 stands rejected as being unpatentable over Kim or Yoshioka, as applied to claim 1, and further in view of U.S. Patent No. 5,656,945 to Cain, for the reasons set forth on pages 8-9 of the Office Action;

(vi) Claims 14 stands rejected as being unpatentable over Kim or Yoshioka, as applied to claim 1, and further in view of Wood, for the reasons set forth on page 9 of the Office Action;

(vii) Claims 11-13, 18-19 and 21-23 stand rejected as being unpatentable over Kim and Yoshioka, as applied to claim 10, and further in view of Applicant's Admitted Prior Art, for the reasons set forth on pages 10-11 of the Office Action; and

(viii) Claim 20 stands rejected as being unpatentable over Kim and Yoshioka and Applicants Admitted Prior Art, as applied to claim 18, and further in view of Wood, for the reasons set forth on pages 11-12 of the Office Action.

Each of the above obvious rejections is based, in part, on the contention that Kim and/or Yoshioka teaches the elements of claims 1 and 10 (although Examiner's rejection (vii) of claim 18 as applied to claim 10 appears to inadvertently treat claim 18 as dependent from claim 10).

However, as explained above, at the very least, neither Kim nor Yoshioka, singularly or in combination, discloses or suggests the inventions of claims 1, 10 and 18. Moreover, the cited references Wood, Cain, Cheung and Zawaideh, clearly do not cure the deficiencies of Kim or Yoshioka with regard to claims 1, 10 and 18. Thus, the above cited combinations of references fail to establish a *prima facie* case of obviousness against any of the claimed invention.

Accordingly, withdrawal of the rejections under 35 § U.S.C. 103 is respectfully requested.

For the foregoing reasons, the present application is believed to be in condition for allowance. Early and favorable reconsideration of the case is respectfully requested. The Examiner is invited to contact the undersigned if he has any questions or comments in this matter.

Respectfully submitted,



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